PATENT ABSTRACTS OF JAPAN

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(21)Application number : **07-047004**
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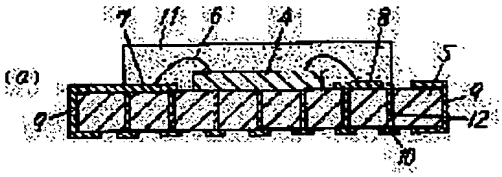
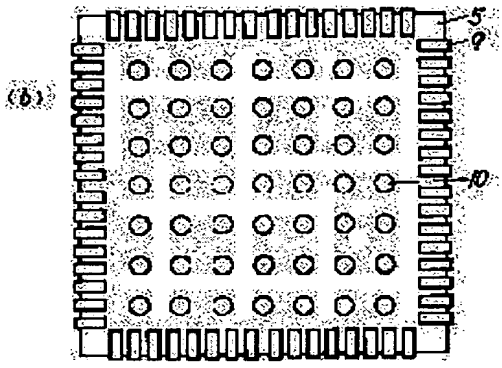
(54) SEMICONDUCTOR DEVICE

(57)Abstract:
PURPOSE: To increase the number of electrodes and cope with the multipin configuration of outer connection electrodes, by using side surface outer connection electrodes and rear surface outer connection electrodes, as the respective mutually independent terminals.
CONSTITUTION: A semiconductor element 4 is electrically connected with electrode pad parts 7, 8 by using connection means like wires 6. The electrode pad 7 is connected with a side surface outer connection electrode 9. The electrode pad 8 is connected with a rear surface outer connection electrode 10. The semiconductor element 4 on a leadless circuit board 5 and wires 6 are resin-sealed with a sealing body 11. Thereby, the number of electrodes can be increased when the number of wirings of the semiconductor element 4 is large, so that multipin configuration is enabled and super multipin structure can be realized.





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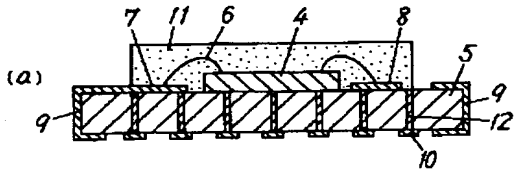
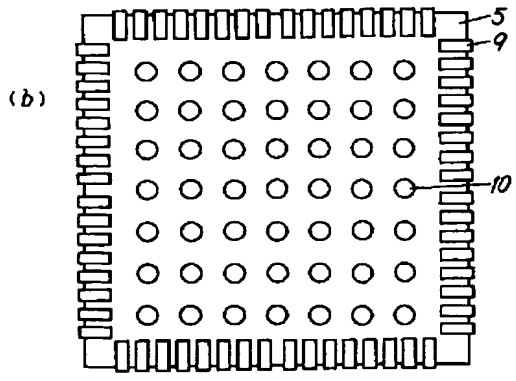
(54)【発明の名称】半導体装置

(57)【要約】
【目的】　小型化、外部接続電極間の狭ピッチ化、多ピン化の要望に応え、基板実装時の接合検査ができる半導体装置を提供する。
【構成】　半導体素子４を搭載したリードレス回路基板５と、半導体素子４とワイヤー６によって電気的に接続される電極パッド部７，８と、電極パッド部７と接続している外部接続用の側面外部接続電極９と、電極パッド部８と接続している外部接続用の裏面外部接続電極１０と、リードレス回路基板５上の半導体素子４、ワイヤー６の領域を樹脂封止した封止体１１とで構成され、半導体素子４の配線数が多くなっても、側面と裏面との両面に外部接続電極を設けているので、多ピン化に十分対応することができ、超多ピン化が実現できる。また側面外部接続電極９と裏面外部接続電極１０とを同時に基板に実装することにより、実装接続強度がより強力となり、接合安定性が向上する。





【特許請求の範囲】

【請求項１】　絶縁性の回路基板と、前記回路基板の表面上に機械的・電気的に載置された半導体素子と、前記回路基板の表面上に設けられた第１の電極パッド部と第２の電極パッド部と、前記半導体素子と前記第１，第２の電極パッド部とを電気的に接続した接続手段と、前記第１の電極パッド部と電気的接続し、前記回路基板の側面領域に設けられた第１の外部接続電極と、前記第２の電極パッド部と前記回路基板の内部において電気的接続し、前記回路基板の裏面領域に配列された第２の外部接続電極と、前記回路基板上の半導体素子の領域を覆った封止体とよりなることを特徴とする半導体装置。

【請求項２】　第１の外部接続電極と第２の裏面外部接続電極とが、それぞれ１対ずつ導体により接続されていることを特徴とする請求項１記載の半導体装置。

【請求項３】　第１の外部接続電極と第２の外部接続電極とが、おのおの電気的に独立した電極であることを特徴とする請求項１記載の半導体装置。

【請求項４】　第１の外部接続電極と第２の外部接続電極とが、一部分、導体により接続されていることを特徴とする請求項１記載の半導体装置。

【発明の詳細な説明】

【０００１】

【産業上の利用分野】本発明は、側面外部接続電極とともに裏面外部接続電極を有する半導体装置に関するものである。

【０００２】

【従来の技術】従来の半導体装置について図面を参照しながら説明する。

【０００３】図２は表面実装型半導体装置（ＱＦＰ）などに見られるパッケージの側面に外部接続電極を有する構造の半導体装置を示す図である。図２（ａ）の側面図，図２（ｂ）の底面図に示すＱＦＰタイプの半導体装置は、半導体素子（図示せず）をその内部に搭載したパッケージ部１の各側辺に外部接続電極２を配列した構造である。前記外部接続電極２は、パッケージ部１内の半導体素子と内部で電気的接続されているものである。

【０００４】また、図３はボールグリッドアレイ（ＢＧＡ）などに見られるパッケージの裏面に外部接続電極を有する構造の半導体装置を示す図である。図３（ａ）の側面図，図３（ｂ）の底面図に示すように、ＢＧＡタイプの半導体装置は、半導体素子（図示せず）をその内部に搭載したパッケージ部１の底面領域に外部接続電極３を配列した構造である。前記外部接続電極３は、パッケージ部１内の半導体素子と内部で電気的接続され、パッケージ部１内で内部引き回しされ、パッケージ部１の底面領域に配列されたものである。

【０００５】

【発明が解決しようとする課題】しかしながら、近年、電子機器の小型化にともない、半導体装置の小型化、外部接続電極と外部接続電極との間の狭ピッチ化の要望が強く、ＱＦＰタイプの半導体装置などのように、パッケージ部側面の外部接続電極がこれまで以上に狭くなると、パッケージ部側面の外部接続電極への接触による検査が非常に困難となってくる。また、ＢＧＡタイプの半導体装置のように、パッケージ裏面の外部接続電極のみの実装では、正しく基板に接合されているのかどうか、外観からの判別が困難である。また、基板実装の際に、パッケージ部側面の外部接続電極のみ、もしくは、パッケージ裏面の外部接続電極のみで実装を行なうと実装接続強度が十分得られていないことがある。さらに、半導体装置の外部接続電極の多ピン化の要望に対して、パッケージ部側面の外部接続電極のみ、もしくは、パッケージ裏面の外部接続電極のみを有する半導体装置では、外部接続電極の数に限界があり、多ピン化に対応できないという課題がある。

【０００６】本発明は、前記課題を解決し、小型化、外部接続電極間の狭ピッチ化、多ピン化の要望に応え、基板実装時の接合検査ができる半導体装置を提供することを目的とするものである。

【０００７】

【課題を解決するための手段】前記課題を解決するために、本発明の半導体装置は、回路基板に対して、側面外部接続電極と裏面外部接続電極の両電極を端子として設けることを特徴とし、側面外部接続電極と裏面外部接続電極の両電極を電気的に独立させたり、または接続したりする構成を有している。

【０００８】

【作用】前記構成により、側面外部接続電極と裏面外部接続電極の両電極をそれぞれ独立させた端子として使用することにより、電極数を増加させ、外部接続電極の多ピン化に対応できる。また側面外部接続電極で検査が困難な場合においても、裏面外部接続電極により容易に検査をすることができ、側面外部接続電極と裏面外部接続電極の両電極を実装することにより、側面から実装外観検査をすることができる。さらに実装接続強度が弱い場合においても側面外部接続電極と裏面外部接続電極の両端子で接続することにより、接続強化することができる。

【０００９】

【実施例】以下、本発明の一実施例について、図面を参照しながら説明する。図１に本実施例の半導体装置を示す。図１（ａ）は本実施例における半導体装置の側面方向の断面図である。図１（ｂ）は本実施例における半導体装置の底面図である。

【００１０】図１において、本実施例の半導体装置は、半導体素子４をその表面上に搭載したリードレス回路基板５と、前記半導体素子４とワイヤー６などの接続手段によって電気的に接続される電極パッド部７，８と、前記電極パッド部７と接続している外部接続用の側面外部

接続電極９と、前記電極パッド部８と接続している外部接続用の裏面外部接続電極１０と、前記リードレス回路基板５上の半導体素子４、ワイヤー６の領域を樹脂封止した封止体１１とで構成されるものである。そして電極パッド部８と裏面外部接続電極１０とは、スルーホール１２によって、リードレス回路基板５内部で引き回しされ、リードレス回路基板５の底面に配列されているものである。前記封止体１１は、樹脂封止手段以外でもよく、キャップ等の封止手段でもよい。また図示するように、一部に電極パッド部７と側面外部接続電極９、裏面外部接続電極１０が接続されている部分が存在しているものである。なお前記リードレス回路基板５は、絶縁性のリードレス回路基板である。

【００１１】以上のような構成により、半導体素子４の配線数が多くなっても、側面と裏面との両面に外部接続電極を設けることができるので、多ピン化に十分対応することができ、超多ピン化が実現できる。また側面外部接続電極９と裏面外部接続電極１０とを同時に基板に実装することにより、実装接続強度がより強力となり、接合安定性が向上する。さらに側面と裏面との両面に外部接続電極を設けることにより、外部接続電極の間隔を狭ピッチ化することなく、回路基板領域に外部接続電極を配列することができる。

【００１２】また、裏面外部接続電極１０だけでなく、側面外部接続電極９も同時に設けて、基板実装した場合、側面からの実装外観検査が可能となり、基板に接合されているのかどうか、外観からの判別が容易となる。

【００１３】なお、前記実施例は、側面外部接続電極９と裏面外部接続電極１０とを一部同時に半導体素子４と接続した例を示したが、半導体素子４の配線数に応じて、側面外部接続電極９と裏面外部接続電極１０とを、各々独立した端子として使用したり、側面外部接続電極

９と裏面外部接続電極１０とをそれぞれ１対ずつ導体である電極パッド部７，８により接続して、側面・裏面の共通端子として使用したり、また側面外部接続電極９と裏面外部接続電極１０とを一部分、電極パッド部７，８により接続して使用してもよい。

【００１４】

【発明の効果】以上説明したように、本発明においては、側面外部接続電極と裏面外部接続電極との両方の電極を用いることにより、半導体素子の配線数の増加に対応し、外部接続電極の多ピン化が実現できる。また基板実装した場合、半導体装置の接合検査を外観から容易にできるとともに、側面外部接続電極と裏面外部接続電極との両方の電極の接合により、実装強度を向上することもできる。

【図面の簡単な説明】

【図１】本発明の一実施例における半導体装置を示す図

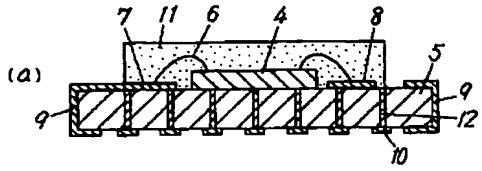
【図２】従来の半導体装置を示す図

【図３】従来の半導体装置を示す図

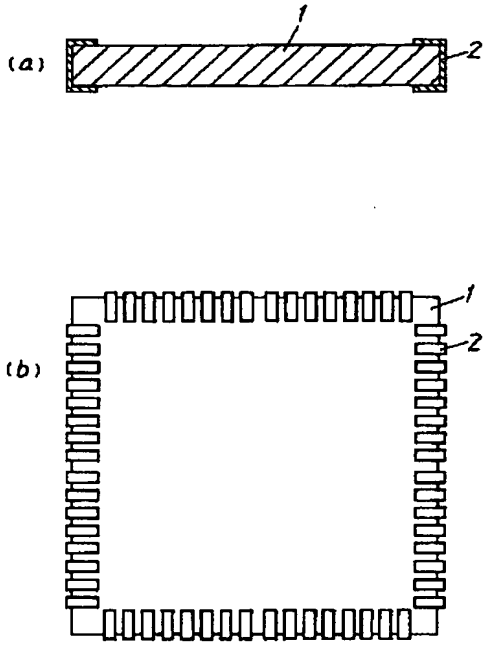
【符号の説明】

１　パッケージ部
２　外部接続電極
３　外部接続電極
４　半導体素子
５　リードレス回路基板
６　ワイヤー
７　電極パッド部
８　電極パッド部
９　側面外部接続電極
１０　裏面外部接続電極
１１　封止体
１２　スルーホール

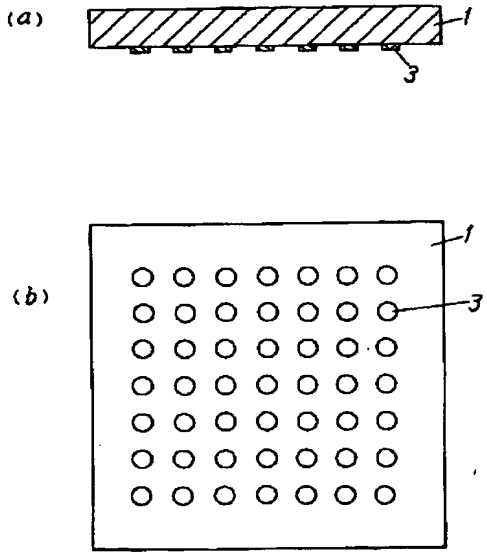
【図１】



【図２】



【図３】



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(54) SEMICONDUCTOR DEVICE

(57)Abstract:

PURPOSE: To increase the number of electrodes and cope with the multipin configuration of outer connection electrodes, by using side surface outer connection electrodes and rear surface outer connection electrodes, as the respective mutually independent terminals.

CONSTITUTION: A semiconductor element 4 is electrically connected with electrode pad parts 7, 8 by using connection means like wires 6. The electrode pad 7 is connected with a side surface outer connection electrode 9. The electrode pad 8 is connected with a rear surface outer connection electrode 10. The semiconductor element 4 on a leadless circuit board 5 and wires 6 are resin-sealed with a sealing body 11. Thereby, the number of electrodes can be increased when the number of wirings of the semiconductor element 4 is large, so that multipin configuration is enabled and super multipin structure can be

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CLAIMS

[Claim(s)]

[Claim 1] The insulating circuit board and the semiconductor device laid mechanically and electrically on the front face of said circuit board, The 1st electrode pad section and the 2nd electrode pad section which were prepared on the front face of said circuit board, The connecting means which connected electrically said semiconductor device and the said 1st and 2nd electrode pad section, The 1st external connection electrode which carried out electrical installation to said 1st electrode pad section, and was prepared in the side-face field of said circuit board, The semiconductor device which carries out electrical installation in said 2nd electrode pad section and interior of said circuit board, and is characterized by consisting of the 2nd external connection electrode arranged to the rear-face field of said circuit board, and a closure object which covered the field of the semiconductor device on said circuit board.

[Claim 2] The semiconductor device according to claim 1 characterized by the 1st external connection electrode and one pair of 2nd rear-face external connection electrode being connected at a time by the conductor, respectively.

[Claim 3] The semiconductor device according to claim 1 characterized by the 1st external connection electrode and the 2nd external connection electrode being electrodes which became independent electrically respectively.

[Claim 4] The semiconductor device according to claim 1 characterized by a part of 1st external connection electrode and 2nd external connection electrode being connected by the conductor.

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2.**** shows the word which can not be translated.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Industrial Application] This invention relates to the semiconductor device which has a rear-face external connection electrode with a side-face external connection electrode.

[0002]

[Description of the Prior Art] It explains referring to a drawing about the conventional semiconductor device.

[0003] Drawing 2 is drawing showing the semiconductor device of the structure of having an external connection electrode on the side face of the package looked at by the surface mount mold semiconductor device (QFP) etc. The semiconductor device of the QFP type shown in the side elevation of drawing 2 (a) and the bottom view of drawing 2 (b) is the structure which arranged the external connection electrode 2 to each **** of the package section 1 which carried the semiconductor device (not shown) in the interior. Electrical installation of said external connection electrode 2 is carried out in the semiconductor device and the interior in the package section 1.

[0004] Moreover, drawing 3 is drawing showing the semiconductor device of the structure of having an external connection electrode at the rear face of the package looked at by the ball grid array (BGA) etc. As shown in the side elevation of drawing 3 (a), and the bottom view of drawing 3 (b), a BGA type semiconductor device is the structure which arranged the external connection electrode 3 to the base field of the package section 1 which carried the

semiconductor device (not shown) in the interior. Electrical installation of said external connection electrode 3 is carried out in the semiconductor device and the interior in the package section 1, and internal leading about is carried out within the package section 1, and it is arranged to the base field of the package section 1.

[0005]

[Problem(s) to be Solved by the Invention] However, if the request of the miniaturization of a semiconductor device and the formation of a ** pitch between an external connection electrode and an external connection electrode is strong and the external connection electrode of a package section side face becomes narrower than the former like a QFP type semiconductor device with the miniaturization of electronic equipment, inspection by the contact to the external connection electrode of a package section side face will become very difficult in recent years. Moreover, distinction from an appearance is difficult like a BGA type semiconductor device whether it is correctly joined to the substrate in mounting of only the external connection electrode on the rear face of a package. Moreover, in the case of substrate mounting, if only the external connection electrode of a package section side face mounts only with the external connection electrode on the rear face of a package, mounting connection resilience may not be obtained enough. Furthermore, to the request of the formation of many pins of the external connection electrode of a semiconductor device, only the external connection electrode of a package section side face has a limitation in the number of external connection electrodes in the semiconductor device which has only an external connection electrode on the rear face of a package, and has the technical problem that it cannot respond to many pin-ization.

[0006] This invention solves said technical problem and aims at offering the semiconductor device which can perform junction inspection at the time of substrate mounting in response to the request of a miniaturization, the external connection inter-electrode formation of a ** pitch, and the formation of many pins.

[0007]

[Means for Solving the Problem] In order to solve said technical problem, the semiconductor device of this invention is characterized by preparing the two electrodes of a side-face external connection electrode and a rear-face external connection electrode as a terminal to the circuit board, and has the configuration made become independent electrically the two electrodes of a side-face external connection electrode and a rear-face external connection electrode or connected.

[0008]

[Function] By said configuration, by using it as a terminal which made the two electrodes of a side-face external connection electrode and a rear-face external connection electrode become independent, respectively, the number of electrodes is made to increase and it can respond to many pin-ization of an external connection electrode. Moreover, with a side-face external connection electrode, when inspection is difficult, it can inspect easily with a rear-face external connection electrode, and mounting visual inspection can be carried out from a side face by mounting the two electrodes of a side-face external connection electrode and a rear-face external connection electrode. When mounting connection resilience is still weaker, connection strengthening can be carried out by connecting by the both-ends child of a side-face external connection electrode and a rear-face external connection electrode.

[0009]

[Example] Hereafter, one example of this invention is explained, referring to a drawing. The semiconductor device of this example is shown in drawing 1 . Drawing 1 (a) is the sectional view of the direction of a side face of the semiconductor device in this example. Drawing 1 (b) is the bottom view of the semiconductor device in this example.

[0010] The lead loess circuit board 5 to which the semiconductor device of this example carried the semiconductor device 4 on the front face in drawing 1 , The electrode pad sections 7 and 8 electrically connected with said semiconductor device 4 by connecting means, such as a wire 6, The side-face external

connection electrode 9 for external connection linked to said electrode pad section 7, It consists of a rear-face external connection electrode 10 for external connection linked to said electrode pad section 8, and a closure object 11 which carried out the resin seal of the semiconductor device 4 on said lead loess circuit board 5, and the field of a wire 6. And the electrode pad section 8 and the rear-face external connection electrode 10 are taken about by the through hole 12 in the lead loess circuit board 5 interior, and are arranged on the base of the lead loess circuit board 5. Except a resin seal means is sufficient as said closure object 11, and closure means, such as a cap, are sufficient as it. Moreover, the part by which the electrode pad section 7, the side-face external connection electrode 9, and the rear-face external connection electrode 10 are connected to the part exists so that it may illustrate. In addition, said lead loess circuit board 5 is the insulating lead loess circuit board.

[0011] By the above configurations, since an external connection electrode can be prepared in both sides of a side face and a rear face even if the number of wiring of a semiconductor device 4 increases, it can respond to many pin-ization enough and super-** pin-ization can be realized. Moreover, by mounting the side-face external connection electrode 9 and the rear-face external connection electrode 10 in a substrate at coincidence, mounting connection resilience becomes more powerful and junction stability improves. An external connection electrode can be arranged to a circuit board field, without forming spacing of an external connection electrode into a ** pitch by furthermore preparing an external connection electrode in both sides of a side face and a rear face.

[0012] Moreover, when not only the rear-face external connection electrode 10 but the side-face external connection electrode 9 is formed in coincidence and carries out substrate mounting, the mounting visual inspection from a side face becomes possible, and distinguishing from an appearance becomes easy whether it is joined to the substrate.

[0013] In addition, although said example showed the example which connected the side-face external connection electrode 9 and the rear-face external

connection electrode 10 with the semiconductor device 4 in part at coincidence It responds to the number of wiring of a semiconductor device 4. The side-face external connection electrode 9 and the rear-face external connection electrode 10 It connects by the electrode pad sections 7 and 8 which became independent respectively and which it is used as a terminal or are conductors one pair at a time, respectively about the side-face external connection electrode 9 and the rear-face external connection electrode 10. It may be used as a common terminal of a side face and a rear face, and the side-face external connection electrode 9 and the rear-face external connection electrode 10 may be used, connecting by the electrode pad sections 7 and 8 in part.

[0014]

[Effect of the Invention] As explained above, in this invention, by using the electrode of both a side-face external connection electrode and a rear-face external connection electrode, it corresponds to the increment in the number of wiring of a semiconductor device, and many pin-ization of an external connection electrode can be realized. Moreover, when substrate mounting is carried out, while being able to make junction inspection of a semiconductor device easy from an appearance, mounting reinforcement can also be improved by junction of both electrodes to a side-face external connection electrode and a rear-face external connection electrode.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1] Drawing showing the semiconductor device in one example of this invention

[Drawing 2] Drawing showing the conventional semiconductor device

[Drawing 3] Drawing showing the conventional semiconductor device

[Description of Notations]

1 Package Section

2 External Connection Electrode

3 External Connection Electrode

4 Semiconductor Device

5 Lead Loess Circuit Board

6 Wire

7 Electrode Pad Section

8 Electrode Pad Section

9 Side-Face External Connection Electrode

10 Rear-Face External Connection Electrode

11 Closure Object

12 Through Hole

[Translation done.]

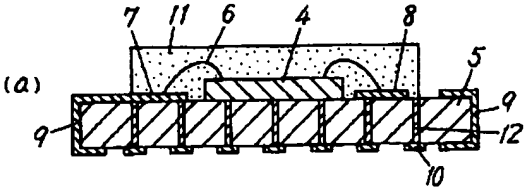
* NOTICES *

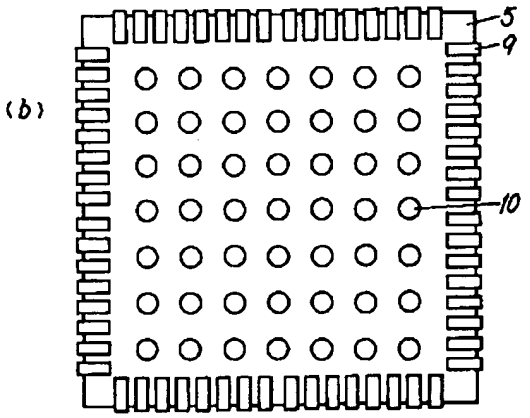
2.**** shows the word which can not be translated.

3.In the drawings, any words are not translated.

DRAWINGS

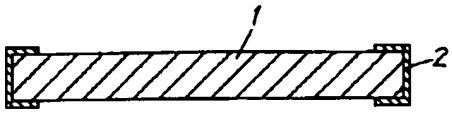
[Drawing 1]



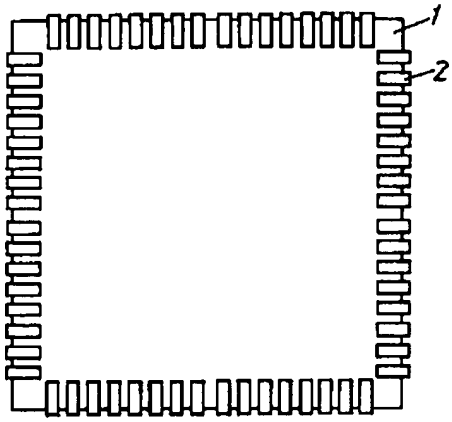


[Drawing 2]

(a)

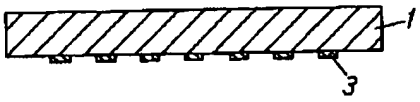


(b)



[Drawing 3]

(a)



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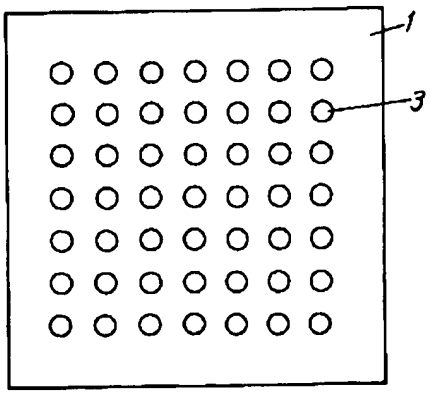

[Translation done.]